APPLICATION

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TITLE: FABRICATION OF A FERAM CAPACITOR USING A NOBLE METAL HARDMASK

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# Fabrication of a FeRAM Capacitor Using a Noble Metal Hardmask

## Field of the Invention

The present invention relates to a hardmask used to etch ferroelectric capacitors.

## Background of the Invention

Ferroelectric capacitors are often used in FeRAMs. The ferroelectric capacitors are etched in one or more steps. FIGURE 1 illustrates a two-step prior-art process for etching a ferroelectric capacitor. A top electrode (TE) 101 and an underlying ferroelectric layer 103 are patterned by a first etching step as shown in FIGURE 1 (b). An underlying bottom electrode (BE) 105 is patterned by a second etching step as shown in FIGURE 1 (c).

Turning to FIGURE 1(a), a wafer stack 100 is illustrated. Sandwiched between the top electrode 101 and the bottom electrode 105 is the ferroelectric layer 103. The top and bottom electrodes 101, 105 are composed of a noble metal such as Platinum or Iridium. The ferroelectric layer 103 can be formed of PZT, for example. The top electrode 101, ferroelectric layer 103, and bottom electrode 105 are supported by a substrate 109.

A first lithographic step is performed whereby a first hardmask 107, often composed of TEOS, is applied on the top electrode 101 for etching the top electrode during the first etching step. During the first etching step the exposed areas of the top electrode 101 and the ferroelectric layer 103 are etched away following the pattern of the first hardmask 107.

The thickness of the first hardmask 107 is chosen according to the selectivity between the hardmask 107 material and the material of the top electrode 101 and the ferroelectric layer 103. The hardmask 107 must be thick enough so that the top electrode and ferroelectric layer are patterned before the hardmask is etched away, exposing the top electrode. Typically, the hardmask must be thicker than the stack itself, resulting in an etching process sensitive to small changes in composition and stack thickness. If the hardmask is thick compared to the capacitor thickness, unwanted residues are easily formed on

the sidewalls. These undesirable effects are common when silicon dioxide (TEOS) is used for the first hardmask 107 and Pt is used for the top electrode.

After etching the top electrode 101 and the ferroelectric layer, a second lithographic step is performed whereby a second hardmask 111 is applied over remaining portions of the first hardmask 107, top electrode 101, ferroelectric layer 103, and bottom electrode 105. FIGURE 1 (b) shows the stack 100 following the deposition of the second hardmask 111.

During the second etching step the exposed areas of the bottom electrode 105, and sometimes some of the substrate 109, are etched away following the pattern of the second hardmask 111. The bottom electrode 105 also includes a barrier layer which is etched along with the bottom electrode 105. FIGURE 1 (c) shows the stack 100 following the second etching step.

The hardmasks used for both the first and second etching steps cause unwanted residues ("fences") clinging to the sidewalls. Moreover, the thick hardmask layers result in overly thick capacitors. The steps for depositing the hardmask layers also adds complexity to the fabrication process.

A hardmask that would allow the simplified fabrication of a relatively thin capacitor stack, with fewer undesirable residues, would be beneficial.

## Summary of the Invention

The present invention uses the top electrode as a noble metal hardmask resulting in simplification of the fabrication process, a thinner capacitor stack and reduced fences.

In general terms, the invention is a ferroelectric capacitor which is fabricated using a noble metal hardmask and also the method for fabricating the capacitor using the noble metal hardmask. A hardmask is deposited on a top electrode of a capacitor stack comprising a ferroelectric layer sandwiched between the top electrode and a bottom electrode. The top electrode is patterned according to the pattern of the hardmask by etching at a first temperature. The top electrode serves as a hardmask and the ferroelectric layer is patterned according to the pattern of the top electrode at a second temperature lower than the first temperature, resulting in the top electrode

having sidewalls beveled relative to a top surface of the top electrode etching. The bottom electrode is etched at a third temperature to form the capacitor.

Brief Description of the Figures

Further preferred features of the invention will now be described for the sake of example only with reference to the following figures, in which:

FIGURES 1a - 1c shows a prior-art process for etching a ferroelectric capacitor.

FIGURE 2 shows a capacitor stack, along with a hardmask deposited on a top electrode, for processing according to the present invention.

FIGURES 3a and 3b show the capacitor stack after etching of the top electrode using the hardmask.

FIGURE 4 shows the capacitor stack following etching of a ferroelectric layer using the top electrode as a hardmask.

FIGURE 5 shows the optional encapsulation of the capacitor stack with another hardmask.

FIGURES 6a and 6b show the capacitor stack after patterning of the bottom electrode.

FIGURE 7 is a flowchart illustrating the method for fabricating the capacitor stack of FIGURES 6a and 6b.

Detailed Description of the Embodiments

The method steps for using a metal hardmask to fabricate a capacitor are described by the flow-chart of FIGURE 7. FIGURES 2-6 schematically illustrate the process for etching a ferroelectric capacitor using a metal hardmask. The present invention takes advantage of the relatively more rapid etching of the ferroelectric layer than the top electrode at lower temperatures, allowing the top electrode to serve as a hardmask.

FIGURE 2 shows a wafer stack 200. Sandwiched between a top electrode 203 and a bottom electrode 205 is a ferroelectric layer 207. In this illustrative example the top and bottom electrodes 101, 105 are composed of the noble metal Platinum (Pt), and the ferroelectric layer 207 is formed of PZT. The top electrode 203, ferroelectric layer 207, and bottom electrode 205 form a capacitor 202 which is supported by a substrate 209.

A first lithographic step is performed whereby a TE hardmask 201 is deposited on the top electrode 203 (step 701 of FIGURE 7). The TE hardmask 201 is used for etching the top electrode. In the present example the TE hardmask 201 is formed from TEOS.

During a first etching step (steps 703) the exposed areas of the top electrode 203 are etched away following the pattern of the TE hardmask 201. The noble metal forming the top electrode 203 is etched at a high temperature T1. For Pt a suitable temperature during the etching of the top electrode 203 at steps 703 is between 250-400degC. The energy to heat the wafer stack 200 is commonly supplied by a direct contact with a heated electrostatic chuck. The high temperature is required to create volatile elements for the noble metal.

The etching can be performed until the hardmask 201 is completely etched away (see FIGURE 3a and step 703a) or the etching can be performed so that some of the hardmask 201 remains to cover the top electrode 203 (see FIGURE 3b and step 703b). The present invention differs from the prior art in that the ferroelectric layer 207 is not completely etched away at this step. The etching is stopped when the metal layer 203 is substantially removed from the ferroelectric 207 over the regions not protected by the top electrode 203.

Next, at step 705 the temperature of the wafer is reduced to reach an etching regime where the volatility of the noble metal forming the metal layer 203 is reduced. The etch rate for the noble metal decreases faster with temperature than the ferroelectric layer. The criteria for the required temperature reduction is the selectivity between the ferroelectric layer and the top electrode hardmask (TE). The temperature of the wafer stack 200 and thickness of the top electrode 203 must be such that in the subsequent etching step the ferroelectric is etched away and patterned by the top electrode 203 before the top electrode 203 is completely etched away. For the embodiment in

which the top electrode 203 is formed from Pt and the ferroelectric layer 207 is formed from PZT, the temperature should be reduced from the 250-400degC temperature by approximately 50-100degC (resulting in a range of lower temperatures from approximately 150-350degC). A preferred temperature range is from 150-250degC. The temperature change can be achieved by moving the wafer 200 from an etching chamber having the higher temperature T1 to an etching chamber having a lower temperature T2 at the step 705.

At step 707 the etching of the ferroelectric layer 207 proceeds at the lower temperature T2 until the ferroelectric layer 207 is patterned by the top electrode 203 to expose the bottom electrode 205 as shown in FIGURE 4. The etching step 707 can also be continued until there is an overetch into the bottom electrode 205. As can be seen from FIGURE 4, the top electrode 203 is eroded during this etching. At the low temperature T2, this leads to faceting of the Pt hardmask top electrode 203. Sidewalls 204 (see FIGURE 4) of the top electrode 203 are beveled relative to a top surface of the top electrode 206. Here "bevel" is defined as "the angle or inclination of a line or surface that meets another at any angle but 90°". Due to the dominating physical component during this etching step, the crystal symmetry of the Pt material leads to this characteristic shape (a tapered shape having a facet angle which can be approximately 60degrees) of the noble metal hardmask top electrode 203.

An optional step 709 is then performed wherein the capacitor 102 is enclosed by a second hardmask, or encapsulation layer 211 as illustrated in FIGURE 5. The encapsulation layer 211 can be composed of TEOS, for example.

Next, a step 711 is performed wherein the bottom electrode is patterned at a suitable temperature T3 which, in some cases, is the same as either T1 or T2.

For the case when the optional step 709 is performed first to enclose the capacitor 102, the encapsulation layer 211 protects the top electrode 203 and ferroelectric layer 207 while the bottom electrode 205 is patterned. FIGURE 6a shows the wafer stack 200 following the etching of the bottom electrode 205.

For the case when step 709 is not performed, or when in step 711 the encapsulation layer 211 is etched away before the bottom electrode 205 is completely patterned, the top electrode 203 can serve as a hardmask for etching the bottom electrode 205. FIGURE 6b shows the wafer stack 200 following the etching of the bottom electrode using the top electrode 203 as the hardmask. For this case, the initial thickness of the top electrode 203 in FIGURE 2 must be enough so that the top electrode 203 is not etched away completely and can serve as a hardmask during the etching of the ferroelecric layer (step 707) and the bottom electrode (step 711).

In step 711 the etching of the bottom electrode 205 can continue so that there is an overetch into the underlying substrate 209.

The present invention results in decreased sidewall deposition (decreased "fences") during capacitor etching. The uniformity of the thickness of the ILD (inter layer dielectric) layer is improved. Also, etching and filling of TW and VO contacts through the wafer stack 200 becomes more reliable and more controllable.

Although the invention has been described above using particular embodiments, many variations are possible within the scope of the claims, as will be clear to a skilled reader. For example, the top and bottom electrodes 101, 105 can be composed of noble metals other than Platinum (Pt), such as Ir, Pd or Rh. Also, rather than using TEOS for the TE hardmask 201 and encapsulation layer 211, other materials suitable for etching at the required temperatures can be used. For example, the hardmask 201 and encapsulation layer 211 can include $Al_2O_3$, Ti, TiN or TiAlN. The etching processes can use plasma etching with $Cl_2$, F or CO based chemistries, for example.